Electronics Project

# 3-bit multiplier

The design for the logic gates is shown in multiplier\_gates file.

The implementation is done using 3 bit adders as shown.

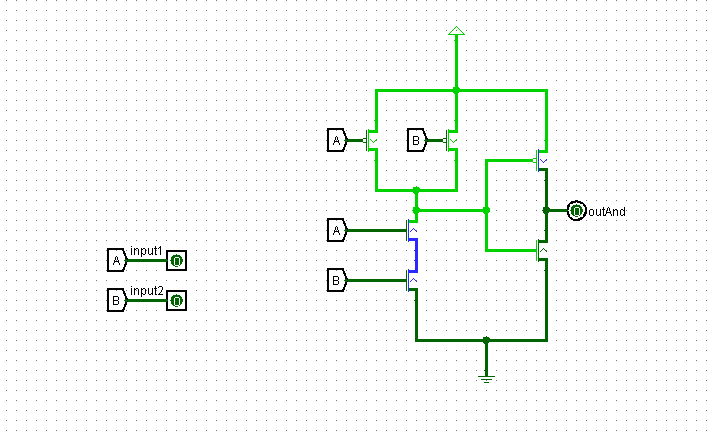
A B on the top left are the 3 bit inputs and result behind them is the output.

A close up of a map

Description automatically generated

Then multiplier\_CMOS contains the design of the same circuit but every element is replaced with it is implementation in CMOS.

## CMOS AND



## CMOS NOT

## 

## CMOS XOR

A close up of text on a white background

Description automatically generated

## CMOS FULL ADDER

A close up of text on a white background

Description automatically generated

## CMOS 3 Bit Adder

A screenshot of text

Description automatically generated

Then the implementation of the up down counter in counter Gates file.

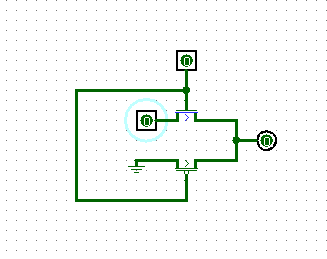
A close up of a map

Description automatically generated

Then the counter pass file contain the implementation for this logic gates in pass-transistor logic.

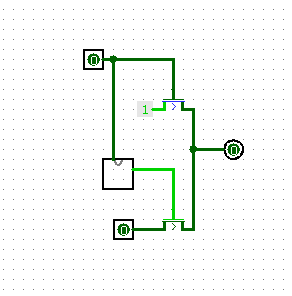
But the master Slave flip flop is in another file as feedback problem in Logisim stops the file from simulation so it is isolated in J-K Flip Flop file

## Pass Transistor AND

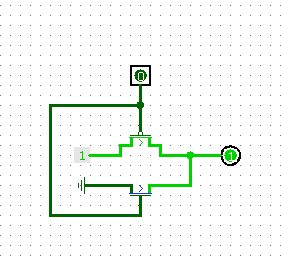


## Pass Transistor OR

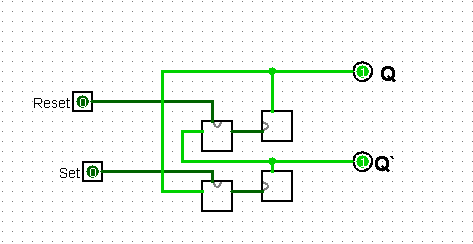
Uses NOT gate



## Pass Transistor NOT



## R-S latch



## J-K master slave FLIP FLOP

